

What is claimed is:

1. A method of creating a circuit assembly, comprising the steps of:

providing a semiconductor substrate, having been provided with at least one active surface region wherein at least one semiconductor circuit has been created, with at least one first electrical point of contact having been provided in said at least one active surface region of said substrate;

providing a first interface created overlying said surface of said semiconductor substrate comprising a first layer of dielectric having openings whereby at least one of said openings is filled with a conductive material that contacts at least one of said at least one electrical contacts provided in said surface of said substrate, thereby creating second electrical contacts in the surface of said first interface;

providing at least one semiconductor die having been provided with active circuits in or on the surface thereof, further having been provided with at least one first contact ball or contact point forming at least one third electrical contact;

providing electrical contact between at least one of said third electrical contacts of said at least one semiconductor die and at least one of said second electrical contacts;

providing an underfill for said at least one semiconductor die, curing said underfill;

depositing a second layer of dielectric over the surface of said at least one semiconductor die, planarizing said deposited second layer of dielectric;

creating at least one via opening penetrating said second layer of dielectric and said first layer of dielectric, exposing at least one of said first electrical contacts provided in said at least one active region in said surface of said substrate;

depositing and patterning a first layer of conductive material over the surface of said second layer of dielectric, filling said at least one via opening created in said second layer and first layer of dielectric with a conductive material, further creating a first interconnect network over the surface of said second layer of dielectric, thereby contacting at least one of said at least one via openings created in said second layer of dielectric, thereby establishing electrical contact between said first interconnect network and at least one of said first electrical contacts in said at least one active region in the surface of said substrate;

providing second contact balls with at least one of said second contact balls contacting said first interconnect network, thereby including at least one of said at least one vias; and

separating said at least one semiconductor device from its surrounding region by die sawing said semiconductor substrate without affecting any interconnect metal that is connected to

said at least one semiconductor device, creating an intermediate semiconductor package.

2. The method of claim 1 creating a complete semiconductor package, comprising the steps of:

providing said intermediate semiconductor package;

providing an interconnect substrate, said interconnect substrate having a first surface and a therewith essentially parallel second surface, with contact pads having been provided in said second surface of said interconnect substrate and contact balls having been provided on said second surface of said interconnect substrate;

connecting at least one of said second contact balls contacting said first interconnect network, thereby including at least one of said at least one vias to at least one of said contact pads provided in said first surface of said interconnect substrate; and

providing an underfill to said intermediate semiconductor package, thereby creating said complete semiconductor package.

3. The method of claim 1 wherein said providing a first interface created overlying said surface of said semiconductor substrate comprises the steps of:

depositing a first layer of dielectric over the surface of said substrate;

creating at least one opening through said first layer of dielectric that aligns with said at least one first electrical point of contact created in the surface of said substrate, exposing the surface of said at least one first electrical point of contact created in the surface of said substrate;

creating a seed layer over the surface of said first layer of dielectric, including the exposed surface of said at least one first electrical point of contact created in the surface of said substrate;

depositing a layer of photoresist over the surface of said seed layer;

patterning and developing said layer of photoresist, creating a second pattern of openings in said layer of photoresist that aligns with said at least one first electrical point of contact created in the surface of said substrate;

plating a layer of solder, creating solder contact plugs that align with and contact said at least one first electrical point of contact created in the surface of said substrate;

planarizing said layer of plated solder down to the surface of said layer of patterned and developed photoresist using methods of Chemical Mechanical Planarization; and

removing said patterned and developed layer of photoresist from above the surface of said substrate, exposing said surface of said seed layer, further exposing portions of said plated solder that protrude above said first layer of dielectric.

4. The method of claim 1 wherein said providing electrical contact between at least one of said third electrical contacts of said at least one semiconductor die and at least one of said second electrical contacts comprises the steps of:

applying a flux coating to said third electrical contacts;

selecting and placing said at least one semiconductor die such that said third electrical contacts align with and make contact with said at least one of said second electrical contacts; and

applying reflow to said third electrical contacts.

5. The method of claim 4 with an additional step of removing excess solder flux by a process of surface cleaning.

6. The method of claim 1 wherein said creating at least one via opening penetrating said second layer of dielectric and said first layer of dielectric uses methods of laser drill or photolithography.

7. The method of claim 1 wherein said creating a first interconnect network over the surface of said second layer of dielectric comprises the steps of:

sputtering a layer of seed metal over the surface of said second layer of dielectric, said seed layer to serve as plating base for said first interconnect network;

depositing a layer of photoresist over the surface of said sputtered layer of seed metal;

patterning and etching said layer of photoresist in preparation for semi-additive plating of said first interconnect network, whereby said pattern created in said layer of photoresist is a reverse pattern of said first interconnect network;

performing semi-additive plating of said first interconnect network;

removing said layer of patterned photoresist from above the surface of said second layer of dielectric; and

wet etching said plating base, removing said plating base where the plating base is not covered with said semi-additive plating, thereby creating said first interconnect network.

8. The method of claim 1 wherein said providing second contact balls comprises the steps of:

depositing a layer of photoresist over the surface of said second layer of dielectric, thereby including the surface of said at least one via and the surface of said first interconnect network;

patterning and etching said layer of photoresist, creating openings in said layer of photoresist that align with said at least one via and the surface of said first interconnect network;

plating a layer of solder over the surface of said layer of photoresist, creating solder contacts with said at least one via and the surface of said first interconnect network;

removing said patterned layer of photoresist from the surface of said second layer of dielectric; and

applying reflow to said created solder contacts.

9. A method of forming a semiconductor device package, said method providing for the simultaneous packaging of more than one semiconductor device after which the semiconductor device package can be separated into individually packaged semiconductor devices that can further be used for additional packaging, said method comprising the steps of:

providing a silicon substrate and at least one semiconductor device, whereby at least one active surface area comprising active devices having points of electrical contact thereto has been provided in the surface of said substrate and points of

electrical contact having been provided in the surface of said at least one semiconductor device;

providing a first interface between said at least one semiconductor device and said at least one active surface area in the surface of said substrate, a first array of contact balls or contact pins within said first interface providing electrical contact between said points of electrical contact provided in said at least one semiconductor device and points of electrical contact provided in said at least one active surface area in the surface of said substrate;

mounting at least one semiconductor device over at least one active surface area provided in the surface of said substrate;

providing underfill for said at least one semiconductor device;

depositing a layer of dielectric over said at least one semiconductor device, planarizing said layer of dielectric;

creating at least one via in said layer of dielectric and in said first interface, said at least one via exposing at least one contact point provided at least one active area in the surface of said substrate;

creating a first network of interconnect lines on the surface of said layer of dielectric, said first network of interconnect lines contacting at least one of said contacts provided in said at least one active area in the surface of said

substrate through said at least one via created in said layer of dielectric;

attaching a second array of contact balls to said first network of interconnect lines including said at least one via created in said layer of dielectric and said first interface;

singulating said at least one semiconductor device by sawing said substrate, creating at least one partially completed singulated semiconductor having at least one contact ball belonging to said second array of contact balls;

providing an interconnect substrate that has a first surface and a second surface with at least one bonding pad provided in said second surface of said interconnect substrate and a third array of contact balls comprising at least one contact ball provided in said first surface of said interconnect substrate;

connecting at least one of said at least one bonding pad in said second surface of said interconnect substrate with said at least one contact ball of said second array of contact balls; and

providing an underfill for said at least one partially completed singulated semiconductor, completing the formation of said semiconductor device package.

10. The method of claim 9 wherein said providing a first interface between said at least one semiconductor device and said substrate comprises the steps of:

depositing a first layer of dielectric over the surface of said substrate;

patterning and etching said first layer of dielectric, creating openings in said layer of dielectric that expose said points of electrical contact in the surface of said substrate;

solder plating said points of electrical contact in the surface of said substrate whereby said patterned and etched layer of dielectric serves as a solder mask; and

planarizing said solder plated points of electrical contact in the surface of said substrate down to the surface of said first layer of dielectric.

11. The method of claim 9 wherein said mounting at least one semiconductor device over at least one active surface area provided in the surface of said substrate comprises the steps of:

flux-coating the surface of said first interface between said at least one semiconductor device and said substrate;

selecting at least one of said at least one semiconductor device;

placing said selected at least one semiconductor device above said silicon substrate whereby said contacts points in said surface of said at least one semiconductor device align with contact points provided in said at least one active surface area in the surface of said substrate;

joining said placed at least one semiconductor device with the surface of said substrate; and

providing reflow between said contacts points in said surface of said at least one semiconductor device and said contact points provided in the surface of said substrate.

12. The method of claim 9 wherein said creating a first network of interconnect lines on the surface of said layer of dielectric comprises the steps of:

sputtering a layer of seed metal over the surface of said layer of dielectric, said seed layer to serve as plating base for said first network of interconnect lines;

depositing a layer of photoresist over the surface of said sputtered layer of seed metal;

patterning and etching said layer of photoresist in preparation for semi-additive plating of said first interconnect network, whereby said pattern created in said layer of photoresist is a reverse pattern of said first interconnect network;

performing semi-additive plating of said first interconnect network;

removing said layer of patterned photoresist from above the surface of said layer of dielectric; and

wet etching said plating base, removing said plating base where this plating base is not covered with said semi-additive plating, thereby creating said first interconnect network.

13. The method of claim 9 wherein said attaching a second array of contact balls to said first network of interconnect lines including said at least one via created in said layer of dielectric comprises the steps of:

creating solder bumps overlying said first network of interconnect lines, including said at least one vias created in said layer of dielectric; and

reflowing said solder bumps.

14. A semiconductor circuit assembly, comprising:

a semiconductor substrate, having been provided with at least one active surface region wherein at least one semiconductor circuit has been created, with at least one first electrical point of contact having been provided in said at least one active surface region of said substrate;

a first interface created overlying said surface of said semiconductor substrate comprising a first layer of dielectric having openings whereby at least one of said openings is filled with a conductive material that contacts at least one of said at least one electrical contacts provided in said surface of said

substrate, thereby creating second electrical contacts in the surface of said first interface;

at least one semiconductor die having been provided with active circuits in or on the surface thereof, further having been provided with at least one first contact ball or contact pin forming at least one third electrical contact;

electrical contact between at least one of said third electrical contacts of said at least one semiconductor die and at least one of said second electrical contacts;

an underfill for said at least one semiconductor die, said underfill having been cured;

a second layer of dielectric deposited over the surface of said at least one semiconductor die, said deposited second layer of dielectric is planarized;

at least one via opening penetrating said second layer of dielectric and said first layer of dielectric, exposing at least one of said first electrical contacts provided in said at least one active region in said surface of said substrate;

a first layer of conductive material deposited and patterned over the surface of said second layer of dielectric, filling said at least one via opening created in said second layer and first layer of dielectric with a conductive material, further forming a first interconnect network over the surface of said second layer of dielectric, thereby contacting at least one of said at least

one via openings created in said second layer of dielectric, thereby establishing electrical contact between said first interconnect network and at least one of said first electrical contacts in said at least one active region in the surface of said substrate;

second contact balls with at least one of said second contact balls contacting said first interconnect network, thereby including at least one of said at least one vias; and

said at least one semiconductor device separated from its surrounding region by die sawing said semiconductor substrate without affecting any interconnect metal that is connected to said at least one semiconductor device, creating an intermediate semiconductor package.

15. The semiconductor circuit assembly of claim 14 further extended to comprise:

said intermediate semiconductor package;

an interconnect substrate, said interconnect substrate having a first surface and a therewith essentially parallel second surface, with contact pads having been provided in said second surface of said interconnect substrate and contact balls having been provided on said second surface of said interconnect substrate;

at least one of said second contact balls contacting said first interconnect network, thereby including at least one of said at least one vias to at least one of said contact pads provided in said first surface of said interconnect substrate; and

an underfill provided to said intermediate semiconductor package, thereby creating said complete semiconductor package.

16. The semiconductor circuit assembly claim of 14 wherein said first interface created overlying said surface of said semiconductor substrate comprises:

a first layer of dielectric over the surface of said substrate;

openings in said first layer of dielectric that align with said at least one first electrical point of contact created in the surface of said substrate, exposing the surface of said at least one first electrical point of contact created in the surface of said substrate;

a seed layer created over the surface of said first layer of dielectric including said exposed surface of said at least one first electrical point of contact created in the surface of said substrate;

solder contact plugs in said first layer of dielectric that align with and contact said at least one first electrical point

of contact created in the surface of said substrate and that further have been planarized down to the surface of said first layer of dielectric using methods of Chemical Mechanical Planarization; and

a layer of seed metal applied to the surface of said planarized plated solder by blanket depositing said seed metal and etching said seed metal in accordance with a pattern that aligns with said planarized plated solder.

17. The semiconductor circuit assembly of claim 14 wherein said electrical contact between at least one of said third electrical contacts of said at least one semiconductor die and at least one of said second electrical contacts comprises third electrical contacts align with and making contact with said at least one of said second electrical contacts.

18. The semiconductor circuit assembly of claim 14 wherein said first interconnect network over the surface of said second layer of dielectric comprises a layer of seed metal sputtered and patterned over the surface of said second layer of dielectric with semi-additive plating added to this seed layer.

19. The semiconductor circuit assembly of claim 14 wherein said second contact balls comprise a layer of plated solder to which

the step of solder reflow has been applied, creating solder contacts with said at least one via and the surface of said first interconnect network.

20. A semiconductor device package, said semiconductor device package comprising the simultaneous packaging of more than one semiconductor device after which the semiconductor device package can be separated into individually packaged semiconductor devices that can further be used for additional packaging, said semiconductor device package comprising:

a silicon substrate and at least one semiconductor device, whereby at least one active surface area comprising active devices having points of electrical contact thereto has been provided in the surface of said substrate and points of electrical contact having been provided in the surface of said at least one semiconductor device;

a first interface provided between said at least one semiconductor device and said at least one active surface area in the surface of said substrate, a first array of contact balls or contact pins within said first interface providing electrical contact between said points of electrical contact provided in said at least one semiconductor device and points of electrical contact provided in said at least one active surface area in the surface of said substrate;

at least one semiconductor device mounted over at least one active surface area provided in the surface of said substrate;

underfill provided for said at least one semiconductor device;

a layer of dielectric deposited over said at least one semiconductor device, planarizing said layer of dielectric;

at least one via created in said layer of dielectric and in said first interface, said at least one via exposing at least one contact point provided at least one active area in the surface of said substrate;

a first network of interconnect lines created on the surface of said layer of dielectric, said first network of interconnect lines contacting at least one of said contacts provided in said at least one active area in the surface of said substrate through said at least one via created in said layer of dielectric;

a second array of contact balls attached to said first network of interconnect lines including said at least one via created in said layer of dielectric and said first interface;

said at least one semiconductor device having been singulated by sawing said substrate, creating at least one partially completed singulated semiconductor having at least one contact ball belonging to said second array of contact balls;

an interconnect substrate that has a first surface and a second surface with at least one bonding pad provided in said

second surface of said interconnect substrate and a third array of contact balls comprising at least one contact ball provided in said first surface of said interconnect substrate;

at least one of said at least one bonding pad in said second surface of said interconnect substrate connected with said at least one contact ball of said second array of contact balls; and

an underfill provided for said at least one partially completed singulated semiconductor.

21. The semiconductor device package claim 20 wherein said first interface between said at least one semiconductor device and said substrate comprises:

a first layer of dielectric over the surface of said substrate;

openings created in said layer of dielectric that expose said points of electrical contact in the surface of said substrate; and

solder plating applied to said points of electrical contact in the surface of said substrate after which said solder plating is planarized.

22. The semiconductor device package of claim 20 wherein said at least one semiconductor device over at least one active surface area provided in the surface of said substrate comprises:

at least one of said at least one semiconductor device that is placed above and joined with said silicon substrate whereby said contacts points in said surface of said at least one semiconductor device align with contact points provided in said at least one active surface area in the surface of said substrate; and

a solder bump provided between said contacts points in said surface of said at least one semiconductor device and said contact points provided in the surface of said substrate.

23. The semiconductor device package of claim 20 wherein said first network of interconnect lines on the surface of said layer of dielectric comprises:

a first layer of dielectric over the surface of said substrate;

openings in said first layer of dielectric that align with said at least one first electrical point of contact created in the surface of said substrate; and

solder contact plugs in said first layer of dielectric that align with and contact said at least one first electrical point of contact created in the surface of said substrate.

24. The semiconductor device package of claim 20 wherein said second array of contact balls attached to said first network of

MEG00-009

interconnect lines including said at least one via created in said layer of dielectric comprises solder bumps created overlying said first network of interconnect lines, including said at least one vias created in said layer of dielectric.